WHAT IS CLAIMED IS:

1. A semiconductor device, comprising:

a substrate;

an insulating layer formed on the substrate;

a fin formed on the insulating layer and including a plurality of side surfaces and a top surface;

a first gate formed on the insulating layer proximate to one of plurality of side surfaces of the fin; and

a second gate formed on the insulating layer separate from the first gate and proximate to another one of plurality of side surfaces of the fin.

2. The semiconductor device of claim 1 wherein the second gate is formed at an opposite side of the fin from the first gate.

3. The semiconductor device of claim 2, wherein the first and second gates respectively include first and second gate contacts.

4. The semiconductor device of claim 1, further comprising:

a plurality of dielectric layers respectively formed along the plurality of side surfaces of the fin.

5. The semiconductor device of claim 4, wherein the first and second gates respectively abut different ones of the plurality of dielectric layers.

6. The semiconductor device of claim 1, wherein the fin comprises at least one of silicon and germanium.

7. The semiconductor device of claim 1, wherein the insulating layer comprises a buried oxide layer.

8. The semiconductor device of claim 1, further comprising:

a source region and a drain region formed above the insulating layer and adjacent a respective first and second end of the fin.

9. The semiconductor device of claim 1, further comprising:

a dielectric layer comprising at least one of a nitride and an oxide formed over the top surface of the fin.

10. The semiconductor device of claim 9, wherein a top surface of the dielectric layer, a top surface of the first gate, and a top surface of the second gate are substantially coplanar.

11. A method of manufacturing a semiconductor device, comprising:

forming an insulating layer on a substrate;

forming a fin structure on the insulating layer, the fin structure including a first side surface, a second side surface, and a top surface;

forming source and drain regions at ends of the fin structure;

depositing a gate material over the fin structure, the gate material surrounding the top surface and the first and second side surfaces;

etching the gate material to form a first gate electrode and a second gate electrode on opposite sides of the fin; and

planarizing the deposited gate material proximate to the fin.

12. The method of claim 11, further comprising:

implanting impurities in the source and drain regions; and

annealing the semiconductor device to activate the source and drain regions.

13. The method of claim 11, further comprising:

forming a dielectric layer over the top surface of the fin structure.

14. The method of claim 13, wherein the planarizing includes:

polishing the gate material so that no gate material remains above the dielectric layer.

15. The method of claim 11, further comprising:

growing oxide layers on the first side surface and the second side surface of the fin structure.

16. A semiconductor device, comprising:

a substrate;

an insulating layer formed on the substrate;

a conductive fin formed on the insulating layer;

gate dielectric layers formed on side surfaces of the conductive fin;

a first gate electrode formed on the insulating layer, the first gate electrode disposed on a first side of the conductive fin adjacent one of the gate dielectric layers; and

a second gate electrode formed on the insulating layer, the second gate electrode disposed on an opposite side of the conductive fin adjacent another one of the gate dielectric layers and spaced apart from the first gate electrode.

17. The semiconductor device of claim 16, further comprising:

a dielectric cap formed over a top surface of the conductive fin.

18. The semiconductor device of claim 17, wherein neither of the first gate electrode and the second gate electrode extend over the dielectric cap.

19. The semiconductor device of claim 17, wherein top surfaces of the first gate electrode, the second gate electrode, and the dielectric cap are substantially coplanar.

20. The semiconductor device of claim 16, wherein the first gate electrode and the second gate electrode are aligned on opposite sides of the conductive fin and are not electrically connected to each other.